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Docket No.: M4065.0184/P184-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Alan G. Wood et al.

Confirmation No.: 9495

Application No.: 09/930,295

Art Unit: 2815

Filed: August 16, 2001

Examiner: C. C. Chu

For: SEMICONDUCTOR DEVICE PACKAGE AND METHOD

Commissioner for Patents
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CONFIRMATION OF TELEPHONE CONFERENCE

As requested by the Examiner, Applicants submit by facsimile the following listing of claims, which reflects the amendments made during a telephone conference with the Examiner on October 26, 2004. The listing of claims begins on page 2 of this document. As discussed with the Examiner, these amendments place the claims in a better condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions and listings of claims for this application:

Listing of Claims:

Claims 1-24 (Canceled).

25. (Currently amended) A semiconductor device package, comprising:

a semiconductor device having diced edges;

a dielectric substrate having diced edges;

a metal layer having diced edges, said metal layer mounted on a first side of said semiconductor device ~~opposite~~, said dielectric substrate mounted on a second side of said semiconductor device, said first and second sides being opposite to each other;

a ball grid array on said dielectric substrate, said dielectric substrate being located between said semiconductor device and said ball grid array; and

electrical connections between said semiconductor device and said ball grid array, ~~said electrical connections comprising at least one first circuit trace between said ball grid array and said dielectric substrate and at least one wire bond connected between said at least one circuit trace and said semiconductor device,~~

wherein said metal layer has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said metal layer edges, so as to provide said package with aligned edges.

26. (Original) The package of claim 25, wherein said metal layer provides a ground plane for said electrical connections.

Claim 27 (Canceled).

28. (Original) The package of claim 25, wherein said metal layer is arranged to dissipate heat from said semiconductor device.

29. (Original) The package of claim 25, wherein said metal layer comprises copper.

30. (Previously presented) The package of claim 25, wherein said connections comprise wire bonds.

31. (Original) The package of claim 25, wherein said connections comprise conductive vias.

32. (Original) The package of claim 31, wherein said connections further comprise conductive traces on opposite sides of said substrate.

33. (Original) The package of claim 32, further comprising solder bumps on said semiconductor device, said bumps being connected to said traces.

34. (Previously presented) The package of claim 25, further comprising an insulative solder mask for covering said dielectric substrate.

Claims 35-38 (Canceled).

39. (Previously presented) The package of claim 25, wherein the metal layer has a thickness within the range of about 0.13 millimeters to about 0.25 millimeters.

40. (Previously presented) A semiconductor device package, comprising:

a semiconductor device having diced edges;

a dielectric substrate having diced edges over an upper side of said semiconductor device;

a first metal layer having diced edges below a lower side of said semiconductor device;

a ball grid array over said dielectric substrate and on an opposite side of said dielectric substrate than said semiconductor device;

at least one first circuit trace on said upper side of said dielectric substrate and connected to a ball pad;

at least one second circuit trace on said lower side of said dielectric substrate; and

at least one metal-plugged via connecting said at least one first circuit trace to at least one second circuit trace.

41. (Previously presented) The semiconductor package of claim 40, wherein said first metal layer has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said first metal layer edges, so as to provide said package with aligned edges.

42. (Previously presented) The semiconductor package of claim 40, wherein said first metal layer has a thickness within the range of about 0.13 millimeters to about 0.25 millimeters.

43. (Previously presented) The semiconductor package of claim 40, further comprising a second metal layer below a lower side of said first metal layer and on an opposite side of said first metal layer from said semiconductor device.

44. (Previously presented) The semiconductor package of claim 43, wherein said first metal layer has a thickness of about 0.00254 millimeters.

45. (Previously presented) The semiconductor package of claim 43, wherein said second metal layer has a thickness within the range of about 0.13 millimeters to about 0.25 millimeters.

46. (Previously presented) The semiconductor package of claim 43, wherein the second metal layer has diced edges aligned with edges of said first metal layer, said semiconductor device edges, and said dielectric substrate edges.

47. (Currently amended) A semiconductor structure comprising:

a plurality of semiconductor chips formed on a wafer;

a plurality of ball grid arrays mounted on a dielectric substrate such that said plurality of ball grid arrays face away from said wafer, each ball grid array respectively associated with one of said plurality of semiconductor chips on said wafer;

electrical connections between each ball grid array and said associated semiconductor chip; and

a first metal layer attached to a side of said semiconductor wafer opposite said ball grid arrays, said metal layer having sufficient stiffness to enable simultaneous dicing of said wafer and said dielectric substrate to form devices comprising portions of said dielectric substrate having respective chips mounted thereon, said chips, first metal layer, and dielectric substrate portions having aligned, diced edges.

48. (Previously presented) The semiconductor structure of claim 47, wherein the dielectric substrate comprises a thin, flexible film.

49. (Previously presented) The semiconductor structure of claim 48, wherein the dielectric substrate comprises any one of FR-4BT resins, epoxy, polymide, KAPTON, UPLEX, and ceramic material.

50. (Previously presented) The semiconductor structure of claim 47, wherein the electrical connections comprise at least one of wire bonds, bond pads, circuit traces, and ball pads.

51. (Previously presented) The semiconductor structure of claim 47, further comprising a second metal layer located at a lower surface of the first metal layer.

52. (Currently amended) A semiconductor device package, comprising:

a semiconductor device having at least one flip chip bump contact;

a dielectric substrate having a via, said via being filled with a conductive material;

a ball grid array on said dielectric substrate, said dielectric substrate being located between said semiconductor device and said ball grid array;

a metal layer attached to the semiconductor device on a side of said semiconductor device opposite said dielectric substrate, said metal layer having sufficient stiffness to enable the simultaneous dicing of said dielectric substrate and said semiconductor device from a structure comprising a

wafer and a dielectric substrate layer attached thereto, said dielectric substrate and said metal layer having aligned diced edges;

at least one interior trace patterned on a top surface of the substrate;

at least one exterior trace patterned on a bottom surface of the substrate, the at least one interior trace being in contract with the at least one flip chip bump on the surface of the semiconductor device and the at least one exterior trace being connected to the interior trace through the conductively filled via.

Claims 53-55 (Canceled).

56. (Previously presented) The semiconductor device package of claim 52, wherein the conductively filled via has a diameter within the range of approximately 25 microns to approximately 200 microns.

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Respectfully submitted,

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